ACORN ECONET BOARD

UNIT DESCRIPTION

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1. INTRODUCTION

1.1 GENERAL

The Acorn Econet board allows System 2/3/4/5 to be connected to the Econet local area network. The Acorn Econet allows computers to communicate and therefore to share expensive resources such as printers and disc filing systems. The Econet system is primarily intended for use in schools and colleges but also lends itself to many office and business applications.

The Econet is a bus network and transmission of information uses two twisted pairs of wires. Data is transmitted in serial bit form over one pair and the other pair transmits a clock signal which is shared by all stations. All stations on the network have equal status and there is no central controller. The network is therefore tolerant against failure since a failure in one computer still allows other computers to use the network. Access to the network is by carrier sense multiple access with collision detect (CSMA/CD). The network can be 500 metres in length and computers simply tap into the main network cable.

This section describes the main details relevant to the Econet eurocard interface. For installation of an Econet network the user is referred to the Econet system and user manual.

1.2 PRINCIPLES OF OPERATION

The operation of the eurocard board can be divided into six main areas:-
(1) The ADLC control chip – This handles the serializing and deserializing of information for the main CPU. The ADLC also handles such complex functions as automatic flag detection and synchronization, zero insertion and deletion, automatic CRC generation and checking, and idle detection.
(2) The line driver – this is responsible for driving the differential twisted pair data lines.
(3) The line receivers – These take serial differential signals on the clock and data lines for input to the ADLC control chip.
(4) Collision detect circuit – This has a dual purpose. First it indicates when the network data lines are undriven. Second it indicates when a current transmission has interference from other simultaneous transmissions.
(5) Clock valid circuit – This circuit provides an input to the Econet software to indicate the main network clock signal is present.
(6) Station selection – this allows the selection of a unique 8-bit network address for the Econet interface.

Essentially the Econet board is an interface between the parallel Acorn bus and the serial Econet network. The ADLC chip controls much of the serial bit stream needed to implement the Econet protocols. For more information on the ADLC chip the user is referred to the Motorola MC6854 technical manual.

1.3 LEADING PARTICULARS

1.3.1 Mechanical

Construction	:	Single Eurocard printed circuit board.
Size	:	100mm x 160mm

1.3.2 Power supplies

+5V +-5% at 250 mA typically.

1.3.3 Connections

Connectors	:	Double sided Eurocard edge connector to Acorn Bus, TTL signal levels are used, OV to 0.4V = logic '0', +2.4V = logic ' 1'.
		180 Deg. 5 pin Din socket for connection to Econet.

2 CIRCUIT DESCRIPTION

The circuit diagram for the Econet eurocard board is shown in Figure 1.

2.1 STATION IDENTIFICATION AND SELECTION

The network number of each station is set up by hardware links on the eurocard hoard. The links are connected to the octal buffer IC 7 and when this is enabled the CPU is able to read the station ID. The links are in two parallel rows of molex pins and make up an eight bit binary station address from 0-255. Each station on the network must have a unique address. Note station numbers 0 and 255 are reserved and must riot be used. Stations 235 and 254 are normally reserved for the printer server and file server respectively. The Econet software will examine the address of every message on the network and compare it with the hardwired address in its own station. A station number is selected by placing molex links on LK 0 to LK 7. Note LK 0 is the least significant bit and LK 7 is the most significant bit. Place a molex shunt in

the positions that require a '0' bit and leave the other positions empty. Table 1 shows a station with address 205 (decimal) selected.

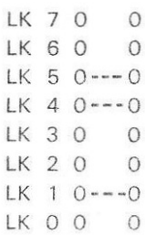


Table 1. Station Selection

2.2 LINE DRIVER

The transmission of data onto the network is via IC1 a 75159 dual differential line driver. The line driver is to the RS 422 specification and can source or sink 40 mA. Differential line techniques ensure both minimal radiation and high noise immunity for the network. The line driver is enabled by Not Request To Send output from the ADLC when Data is transmitted. When disabled or powered down the line driver outputs are high impedence. Stations can therefore be left connected to the network even when they are not in use.

2.3 LINE RECEIVER

The reception of data and clock signals from the network is acomplished using IC2 an LM 319 dual fast comparator. The receive circuits for the clock and data are identical and are designed to give good common mode signal rejection and hysteresis thus providing noise immunity. The reference voltage for the line receivers is two volts provided by R20, R21, and C3. Incoming signal voltages are divided by ten by R4, R5, R8, R11 and R2, R3, R7, R10 for the clock and data respectively. Hysteresis is provided by R15 and R14 for the clock and data signals respectively.

2.4 COLLISION DETECT

The collision detect circuit uses IC4, an LM 319 dual fast comparator. Essentially the circuit is a window comparator and the collision signal is fed into the ADLC Not Clear To Send input. This signal indicates when the data lines are driven by a differential signal greater than one volt. The collision threshold voltage is set by R1. During idle conditions the lines are driven by a 0.6 volts line bias from the network terminator units. This voltage allows the collision detect circuit to indicate the line is free but also feeds a constant stream of binary ones into the ADLC control chip to signal that the line is idle. In the driven state the differential voltage on the data lines is above two volts.

2.5 CLOCK VALID CIRCUIT

The clock valid circuit provides an input to the Not Data Carrier Detect input of the ADLC. The Econet software is therefore able to check that a valid clock exists on the network before transmissions take place. The valid clock condition is sensed using a retriggerable monostable IC 5. The minimum clock rate of the Econet is therefore determined by this monostable time constant and is currently set at 70 kbits/sec.

2.6 ADLC SERIAL CONTROL CHIP

The ADLC control chip is the main component of the Econet board and it contains most of the functions needed to implement the bit oriented protocol of the Econet. The ADLC chip handles such functions as bit serializing and deserializing of data for the main CPU. The ADLC also handles such complex funtions as automatic flag detection and synchronization, zero insertion and deletion, automatic CRC generation and checking, and also idle detection. In addition to relieving the software from such time and code consuming functions the ADLC contains a number of useful input and outputs that simplify the hardware. The Not Request To Send output is used to enable the Econet data line driver, the. Not Clear To Send input is used to detect an undriven line, and the Not Data Carrier Detect is used to detect an absence of clock signal.

2.7 ADDRESS DECODING

The Econet eurocard board takes up five bytes of address space from 1940 to 1944 (hex). The ADLC is mapped from 1940 to 1943 and the station identification is mapped at 1944 (hex).

3. SOFTWARE PARAMETERS

3.1 ECONET SOFTWARE

The Econet software is 4kbytes long and is supplied in EPROM form. On System 5 computers the Econet is conveniently combined with the DOS (Disc Operating System) and is supplied in an 8kbyte EPROM. The EPROM is fitted on the main CPU card and is mapped from E000 to FFFF (hex).

3.2 ECONET ENABLING

Before the Econet can be used on system 5 computers it must be enabled. The enabling action allows the Econet software to initialize the ADLC chip, internal variables, and setup interupt jump addresses. Initialization is achieved using *GO command which can be typed by the user or executed from user software. There are three main addresses depending on what Econet resources are required.

*GOE000 — init. only the Econet low level primitives.
*GOE003 — init. low level, Econet printer, the Econet filing system.
*GOE009 — init. low level, Econet printer, but allow use of a Disc filing system.

4. ECONET BOARD CONNECTIONS

4.1 ECONET BOARD TO ACORN BUS

Pin	Mnemonic	Meaning	I/O
Side A			
1	+5V	+5V Line	I
2	A15	Address Lines	I
3	A14		
6	NRST	Reset	I
7	A8		
8	A7		
9	A6		
10	A5		
11	A4	Address Lines	I
12	A3		
13	A2		
14	A1		
15	A0		
16	D7		
17	D6		
18	D5		
19	D4	Data Lines	I/O
20	D3		
21	D2		
22	D1		
23	D0		
24	A13		
25	A12		
26	A11	Address Lines	I
27	A10		
28	A9		
29	Φ2		
30	R/W	Read/Write Enable	I/O
32	OV	Earth	
Side B			
24	VMA	Valid Memory Address	I
28	IRQ	Interrupt Request	I

4.2 ECONET BOARD TO LINE CONNECTOR

Pin	Mnemonic	Meaning	I/O
1 4	DATA	—	I/O
2	GROUND	—	—
3 5	CLOCK	—	I

5. PARTS LIST

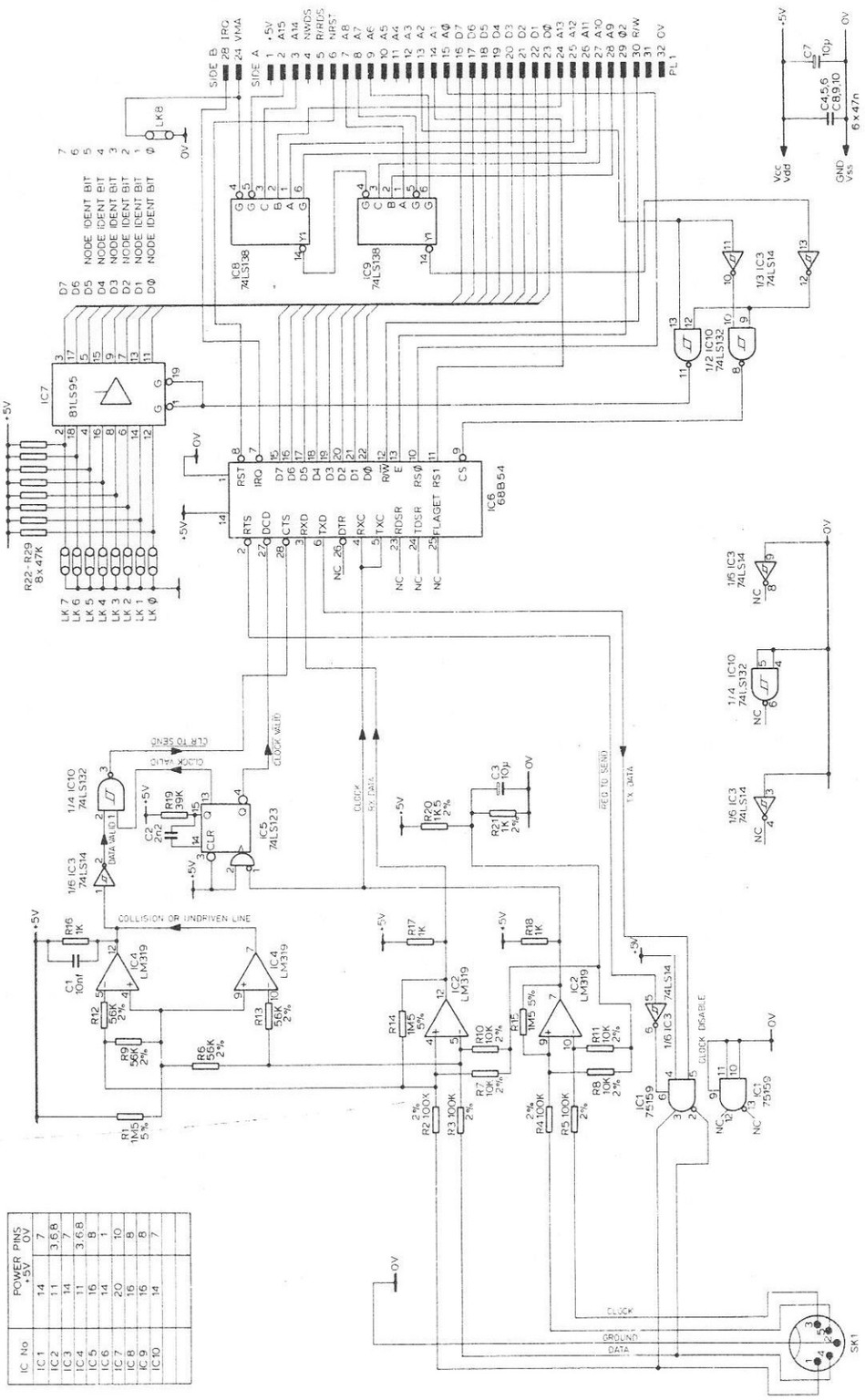
5.1 MECHANICAL PARTS

ITEM	DESCRIPTION	VALUE	QTY.	PART NO.
	Front Panel Kit		1	100,524
	Shunt 2 Way		7	800,070
	Molex Pins 8 Way		2	800,054
	28 Pin IC Socket		1	800,128
	14 Pin IC Socket		3	800,114
	Printed Circuit Board		1	200,024
PL1	Connector, 64 Way		1	800.401
SK1	DIN Socket, 5 Way		1	800,004

5.2 ELECTRICAL PARTS

ITEM	DESCRIPTION	VALUE	QTY.	PART NO.
IC1	Integrated Circuit	75159	1	735,159
IC2/IC4	Integrated Circuit	LM319	2	770,319
IC3	integrated Circuit	74LS14	1	742,014

ITEM	DESCRIPTION	VALUE	QTY.	PART NO.
IC5	Integrated Circuit	74LS123	1	742,123
IC6	Integrated Circuit	68B54	1	706,854
IC7	Integrated Circuit	81LS95	1	738,095
IC8/IC9	Integrated Circuit	74LS138	2	742,138
IC10	Integrated Circuit	74LS132	1	742,132
C1	Capacitor	10nF	1	629,010
C2	Capacitor	2n2	1	629,002
C3/C7	Capacitor, Electrolytic	10µ 1 6V	2	635,100
C4.....C6,C8.....C10	Capacitor	47nF	6	680,001
R1, 14, 15	Resistor	1M5	3	
R2...R5	Resistor 2%	100K	4	505,104
R6, 9, 12, 13	Resistor 2%	56K	4	505,563
R7, 8, 10, 11	Resistor 2%	10K	4	505,103
R16, 17, 18	Resistor	1K	3	500,102
R19	Resistor	39K	1	500,393
R20	Resistor 2%	1K5	1	505,152
R21	Resistor 2%	1K	1	505,102



IC No	POWER PINS +5V	0V
IC1	14	7
IC2	11	3,6,8
IC3	14	7
IC4	11	3,6,8
IC5	16	8
IC6	14	1
IC7	20	10
IC8	16	8
IC9	16	8
IC10	14	7

Figure 1. Econet Eurocard Circuit Diagram